WEST Search History

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L3: Entry 1 of 2 File: USPT Sep 19, 2000

DOCUMENT-IDENTIFIER: US 6122699 A
** See image for Certificate of Correction **
TITLE: Data processing apparatus with bus intervention means for controlling interconnection of plural busses

Detailed Description Text (2):
The present invention provides a data processing apparatus which can improve the net processing speed by substantially parallelly executing the CPU operation and the DMA processing in such a manner that only when a device such as an external RAM (to be described later) shared by the individual processors such as a CPU, DMA processor, and the like is to be accessed, the operation of the one of the CPU and DMA processor is interrupted.

Detailed Description Text (57):
In the present invention, the CPU operation and the DMA processing can be substantially parallelly executed by stopping one of the CPU and the DMA processor only when a device such as an external RAM shared by the individual processors such as the CPU, DMA processor, and the like is to be accessed. The influence of the operation state of the other of the CPU and the DMA processor can be minimized, and the use efficiency of the shared portion can be improved, thereby improving the processing speed.

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L2: Entry 3 of 14 File: USPT Jul 15, 2003

DOCUMENT-IDENTIFIER: US 6594711 B1
TITLE: Method and apparatus for operating one or more caches in conjunction with direct memory access controller

Abstract Text (1):
A data processing apparatus includes a data processor core having integral cache memory and local memory, and external memory interface and a direct memory access unit. The direct memory access unit is connected to a single data interchange port of the data processor core and to an internal data interchange port of the external memory interface. The direct memory access unit transports data according to commands received from the data processor core to or from devices external to the data processing unit via the external memory interface. As an extension of this invention, a single direct memory access unit may serve a multiprocessing environment including plural data processor cores. The data processor core, external memory interface and direct memory access unit are preferably embodied in a single integrated circuit. The data processor core preferably includes an instruction cache for temporarily storing program instructions and a data cache for temporarily storing data. The data processor core requests direct memory access data transfers for cache service.

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L2: Entry 1 of 14 File: USPT Mar 2, 2004

DOCUMENT-IDENTIFIER: US 6701395 B1
TITLE: Analog-to-digital converter that preseeds memory with channel identifier data and makes conversions at fixed rate with direct memory access

Abstract Text (1):
An integrated circuit including a DMA controller, an ADC having a plurality of conversion channels and address and data ports for connection to external memory means, the DMA controller being arranged to read a channel id from the memory means using the address and data port which channel id is representative of one of the said conversion channels, to pass the read channel id to the ADC, to cause the ADC to perform an analog-to-digital-conversion on the conversion channel represented by the channel id, to receive the conversion result from the ADC and to write the conversion result back to the memory means using the address and data ports. Also, an integrated circuit including a microcontroller having an output port, an address valid output line, a latch coupled to the output port, and a latch control fine coupled to the latch control of the latch the microcontroller being operable to present a first range of address bits at its output port, to activate the latch control line to cause the latch to latch the first range of bits, to present a second range of address bits at its output port and to activate the address valid line to indicate that the combination of the first and second ranges present on the latch outputs and the output port respectively, are valid.

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L2: Entry 5 of 14 File: USPT Jun 18, 2002

DOCUMENT-IDENTIFIER: US 6408345 B1
TITLE: Superscalar memory transfer controller in multilevel memory organization

Abstract Text (1):
This invention is a data processing system including a central processing unit executing program instructions to manipulate data, at least one level one cache, a level two unified cache, a directly addressable memory and a direct memory access unit adapted for connection to an external memory. A superscalar memory transfer controller schedules plural non-interfering memory movements to and from the level two unified cache and the directly addressable memory each memory cycle in accordance with a predetermined priority of operation. The level one cache preferably includes a level one instruction cache and a level one data cache. The superscalar memory transfer controller is capable of scheduling plural cache tag memory read accesses and one cache tag memory write access in a single memory cycle. The superscalar memory transfer controller is capable of scheduling plural of cache access state machines in a single memory cycle. The superscalar memory transfer controller is capable of scheduling plural memory accesses to non-interfering memory banks of the level two unified cache in a single memory cycle.

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L2: Entry 7 of 14 File: USPT Oct 30, 2001

DOCUMENT-IDENTIFIER: US 6311234 B1
TITLE: Direct memory access controller with split channel transfer capability and FIFO buffering

Abstract Text (1):
A microprocessor 1 is described which includes a direct memory access (DMA) circuitry 143. DMA 143 is interconnected with a program memory 23 and a data memory 22 and is operational to transfer data to or from these memories. DMA 143 is interconnected with a peripheral bus 110 and thereby to various peripherals internal to microprocessor 1. DMA 143 is also interconnected with an external memory interface 103 and thereby to various external memory circuits and peripherals external to microprocessor 1. An auxiliary channel control circuitry 160 provides DMA transfers by interacting with a peripheral such as host port 150 which has its own address generation circuitry. DMA 143 provides frame synchronization for triggering a frame transfer, or group of transfers. DMA 143 is auto-initialized through registers. DMA action complete pins DMAC0-3 indicate DMA status to external devices. DMA 143 allows for local variability of transfer rates in a split channel mode of operation by allowing a transmit channel to get ahead of a corresponding receive channel by a preselected number of data words.